REMARKS

Claims 1-10, 12-14 and 20-22 are pending in the application. Favorable reconsideration of the application is requested.

Withdrawal of the drawing objection is requested. A review of the specification indicates that there is no intention to have reference character 168 illustrate any feature of the drawings. As set forth on page 7, second paragraph, this was merely the description of an alternative method for implementing the invention. As the particular layer is not the subject matter of a claim, it is not required to show the subject matter in a drawing figure pursuant to 37 C.F.R. § 1.84.

Withdrawal of the rejection of claims 1-3, 5, 7, 9, 12 and 21 under 35 U.S.C. § 102(b) as being anticipated by Khajezadeh (U.S. Pat. No. 4,202,006) is requested.

Claims 1 and 13 have been amended to make it clear that the structure of the second transistor subcollector provides for lateral ballasting. Amended claims 1 and 13 identify the fact that the sheet resistance of the second subcollector is established at 50 Ω/per sq. This means that the current produced from an EST event is uniformly distributed, lowering the current density in the transistor. The lower current density decreases temperature which is the principal agent for producing a failure in a semiconductor device.

Claim 6, original to the application further identifies the relative sheet resistances of each subcollector. By choosing, in accordance with claim 6, a first subcollector sheet resistance below 20 Ω/per sq. and a second collector sheet resistance above 50 Ω/per sq., it is feasible to obtain the effect on the second transistor of lateral ballasting.

Turning now to the cited reference to Khajezadeh (U.S. Pat. No. 4,202,006), a semiconductor integrated circuit is disclosed having a substrate which supports both an integrated injection logic element as well as a bipolar transistor. Two buried pockets 20 and 22 are formed in the substrate 14 with different conductivity modifiers. The bipolar transistor adjacent the first buried pocket 20 exhibits a relatively high breakdown voltage characteristic.

The region 20 is identified as having a sheet resistivity of between 25-30 Ω/per sq. (see col. 3, lines 30-34). The main region 22S has a sheet resistivity of around 10 Ω/per sq. (see col. 3, lines 43-46).

The reference fails to disclose any effects regarding an ESD event, or any effective resistances selected to provide a lateral ballasting of one of the transistors. Accordingly, the structure of independent claims 1 and 13 for producing a lateral ballasting effect is not shown or described in the reference. The reference appears to emphasize the production of a high voltage breakdown device by choosing the foregoing sheet resistivity which can withstand high voltages, not carry a current from an ESD event.

Withdrawal of the rejection of claims 1, 5, 7-9, 12, 20 and 22 under 35 U.S.C. § 102 as being anticipated by Washio et al. (U.S. Pat. No. 4,694,321) is requested. The foregoing reference describes a semiconductor circuit device which has both a bipolar transistor and a integrated injection logic element (IIL). Each of the devices has a respective buried layer formed under the device. In order to inhibit leakage current from the IIL region, the buried layer has a larger GUMMEL number than the buried layer under the bipolar transistor. By using the device structure, the problem of current flowing through the buried layer to the substrate can be decreased without increasing the entire thickness of the component.

The reference fails to disclose any feature which would facilitate the improvement in ESD performance. While a structure having two different buried layers is disclosed, the buried layers are not for the purpose of creating ballasting which will reduce the effects of an ESD current. The specific sheet resistance in claims 1, 6 and 13 used to obtained the ballasting effect is not disclosed in the reference. Accordingly, the reference cannot anticipate or suggest the subject matter of the rejected claims.

Withdrawal of the rejection of claims 1-5, 7-9, 12 and 21 under 35 U.S.C. § 102(b) as being anticipated by Ohkawa et al. (U.S. Pat. No. 5,798,560) is requested. The device disclosed in the Ohkawa et al. (U.S. Pat. No. 5,798,560) reference is an implementation of diodes for recirculating the current of an inductive load. As shown in Fig. 1, when driving an inductive load such as a motor, a reverse voltage is generated which is dissipated through one of two diodes 4.

In carrying out the invention for implementing these diodes, a two stage epitaxial structure is created, where a diode has a greatly reduced leakage current flowing to a substrate. By reducing the leakage current, the integrated circuit does not malfunction from latch-up. By utilizing the structure shown in the reference, these adverse effects for leakage currents are minimized.

The reference fails to disclose anything related to dissipating an EST current. Whereas the present invention provides a subcollector of a specific sheet resistance to provide for a ballasting effect, the cited reference fails to disclose anything other than a diode used to handle the current from the inductive motor load.

Withdrawal of the rejection of claims 1-3, 5, 7, 12 and 21 under 35 U.S.C. § 102(b) as being anticipated by Yamaguchi (JP 63-288055) is requested. The foregoing limitations regarding a subcollector to create ballast effects for decreasing current density from an ESD event are not disclosed in the English abstract of the Yamaguchi (JP 63-288055) reference. Accordingly, this reference as well fails to suggest those limitations of the independent claims 1 and 13 which relate to the sheet density of one subcollector for providing the ballasting to reduce current densities during an ESD event.

Withdrawal of claims 4 and 6 under 35 U.S.C. § 103 as being unpatentable over Khajezadeh (U.S. Pat. No. 4,202,006) is requested. The cited reference, as noted previously, does not provide a subcollector having the required ballasting effect.

Claim 6 is specific to the sheet resistances of the two devices, and define the device which has greater ESD robustness, that having the higher sheet resistance. As noted in the Office Action, Khajezadeh (U.S. Pat. No. 4,202,006) fails to disclose this higher sheet resistance, or the beneficial effects achieved through the subcollector ballasting so that ESD events are safely handled. As the reference does not perform any function related to this feature, it cannot render obvious this subject matter.

Withdrawal of the rejection of claim 10 under 35 U.S.C. § 103 as being unpatentable over Khajezadeh (U.S. Pat. No. 4,202,006), further in view of Hebert et al. (U.S. Pat. No. 6,365,447) is requested. Claim 10 is dependent on claim 1, and carries all the limitations thereof. Accordingly, claim 10 also considered to be allowable.

Withdrawal of the rejection of claims 13 and 14 under 35 U.S.C. § 103 as being unpatentable over Yamaguchi (JP 63-288055), and further in view of Kamins et al. (U.S. Pat. No. 5,633,179), and further in view of Chantre et al. (U.S. Pat. No. 6,436,782) is requested. Claim 13 has been amended to include all those limitations relating to the ballasting effect of the second subcollector. The specific feature for providing the ballasting effect, including a subcollector having a sheet resistance exceeding 50 Ω/per square, remains undisclosed from the combination of references.

In view of the foregoing, where it has been demonstrated that the Applicants provide a new function not disclosed in any of the references, by a subcollector, having been sheet resistance, is considered that the application defines patentable subject matter.

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Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00134-US from which the undersigned is authorized to draw.

Dated: 2/17/04

Respectfully submitted,

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